Amendments to the Specification

Please replace the existing paragraphs with the following amended paragraphs.

[0021] Figure 3 illustrates a block diagram of an embodiment of a processor having logic configured to test and repair two or more memories electrically connected to that processor. The processor 310 connects to multiple memory arrays, such as the first memory 302 through the Nth number of memory ~~332~~330. The processor 310 also connects to a fuse box 314 that stores a concatenated repair signature that repairs all of the memories connected that processor 310. Each of the memories ~~302-330~~302, 330 has one or more redundant components associated with that memory. The processor 310 contains redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each memory. The repair data container may be a fuse box 314. The fuse box 314 stores actual repair signatures for each memory having one or more defective memory cells and dummy repair signatures for each memory with no defective memory cells. The concatenated repair signature may be an aggregation of all the repair signatures for each of the memories connected to that processor 310. The processor 310 contains logic configured to compose a concatenated repair signature for all of the memories ~~302-330~~302, 330 sharing the processor 310 and the fuse box 314. The processor 310 composes a concatenated repair signature in order to store that concatenated repair signature in the fuse box 314. The processor 310 also contains logic configured to decompose the concatenated repair signature to send reconfiguration data into all of the memories ~~302-330~~302, 330 sharing the fuse box 314. The processor 310 also contains logic configured to compress the repair signature when sending bits to be stored in the fuse box 314.

[0023] Referring to figure 3, the reconfiguration data sent by the processor is scanned into the scan chain registers of each memory ~~302-332~~302, 330. The reconfiguration data is the logical 1 and 0 bits that direct each memory on how to utilize their redundant memory cells.

Applicants respectfully submit the typographical correction to the above paragraphs should overcome the objection to the drawings. Applicants also submit a full set of formal drawings with this amendment. As such, please withdraw the objection to the drawings.